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H1S SBA S5 S6A3
U1S S2061 S2088

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None

(58) Field of search
UK CL (Edition K) C7F FARE FARX, H1K KFJ
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(54) **"A method for forming a thin film resistor on an IC wafer"**

(57) A method for forming thin film resistors (4) on a semi-conductor integrated circuit wafer (1) comprises the steps of depositing a resistor layer (14) of silicon chrome for forming the film resistors (4), depositing a protective layer (15) of titanium tungsten over the resistor layer (14), forming a patterned photoresist layer (16) over the protective layer (15) to define the thin film resistors (4), etching to remove the protective layer (15) in areas not protected by the photoresist (16), removing the photoresist (16) and then subjecting the wafer (1) to a radio frequency sputter etch to remove portions of the resistor layer (14) for defining the thin film resistors (4).

Conductors (9) are then formed on the wafer (1) for connecting the thin film resistors (4) together and to other components on the wafer (1).

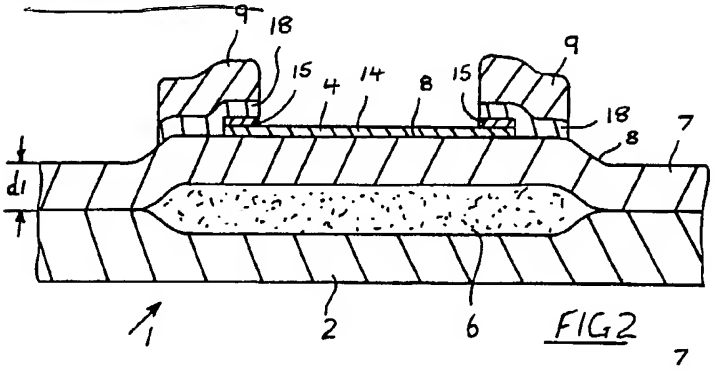

FIG2

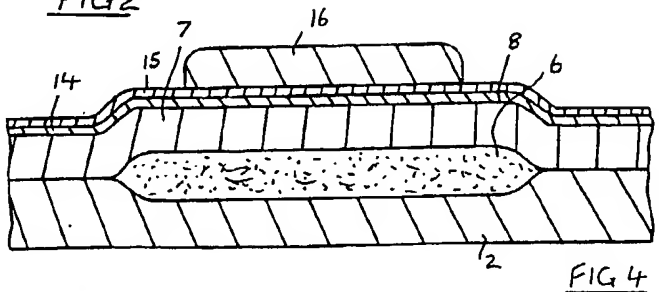

FIG 4

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

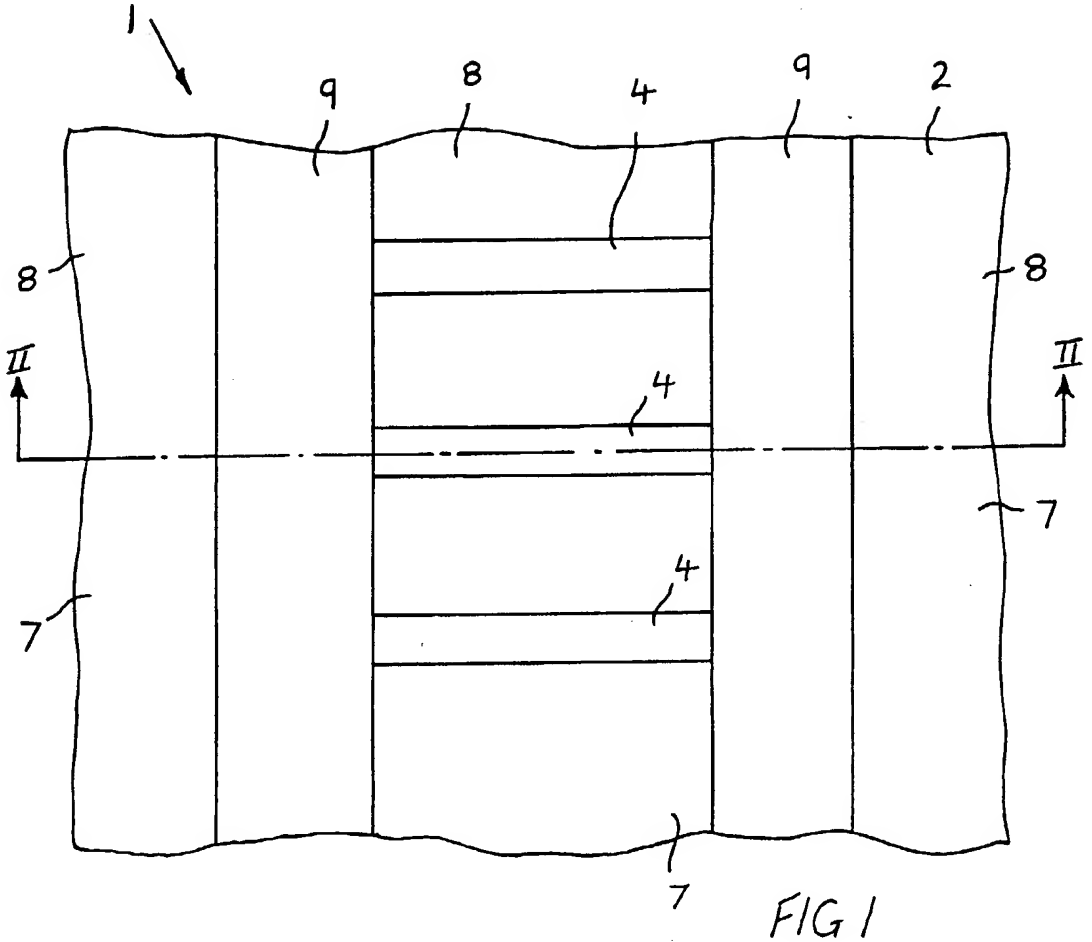

FIG 1

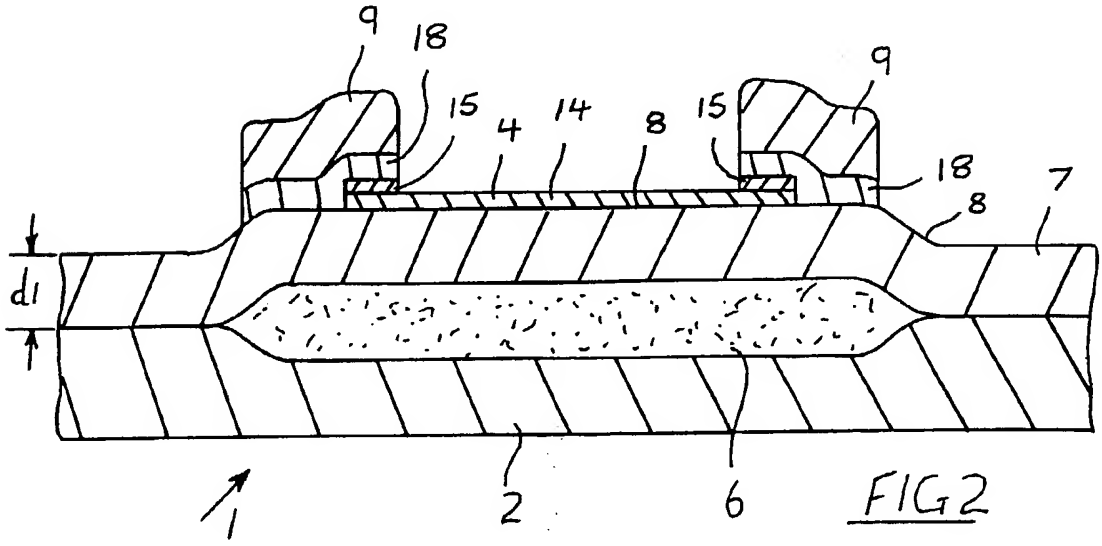

FIG 2

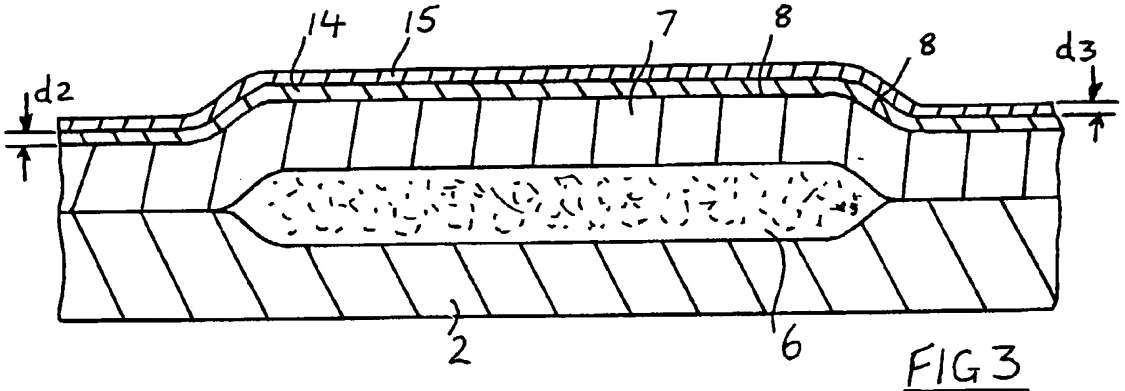

FIG 3

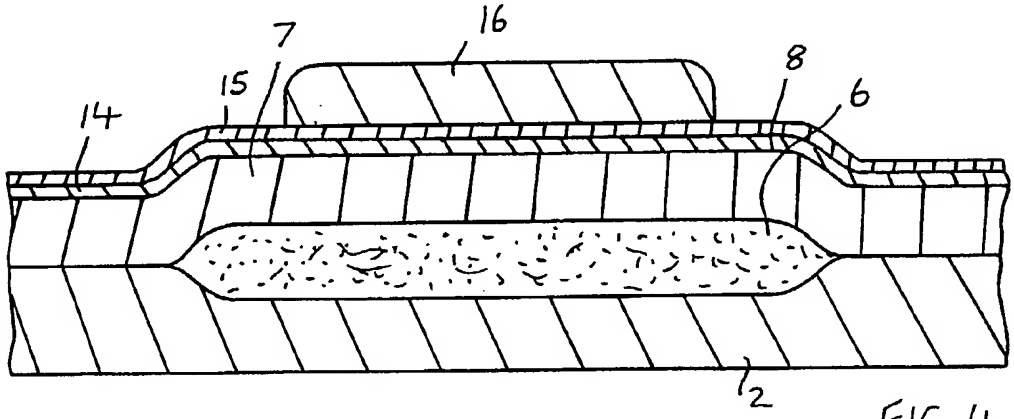

FIG 4

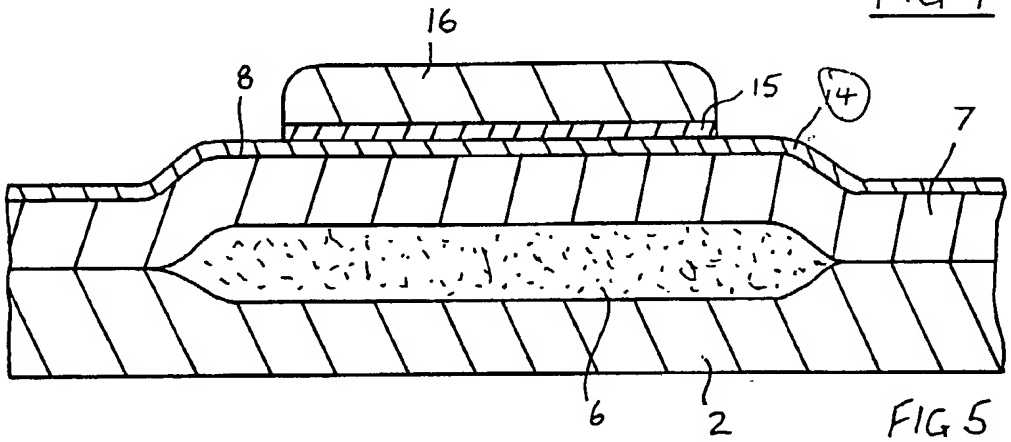

FIG 5

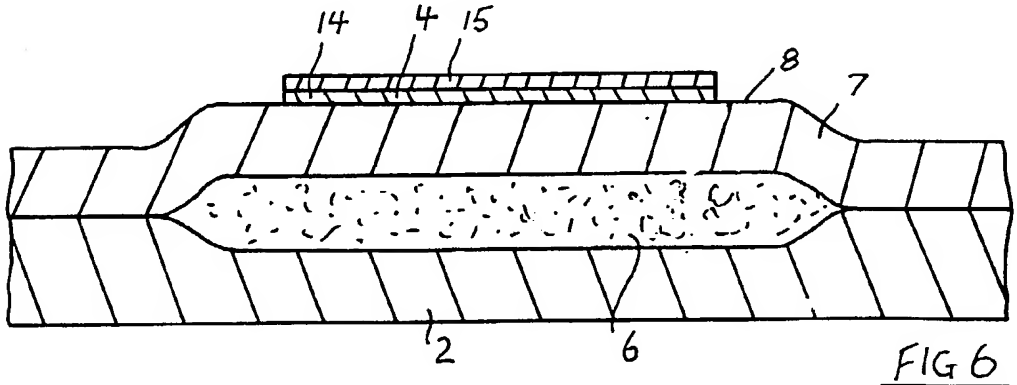

FIG 6

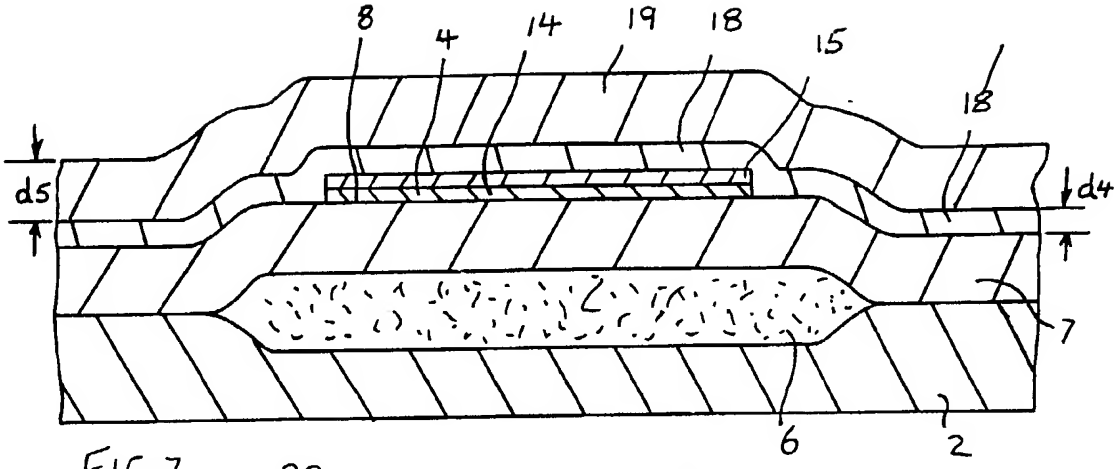

FIG 7

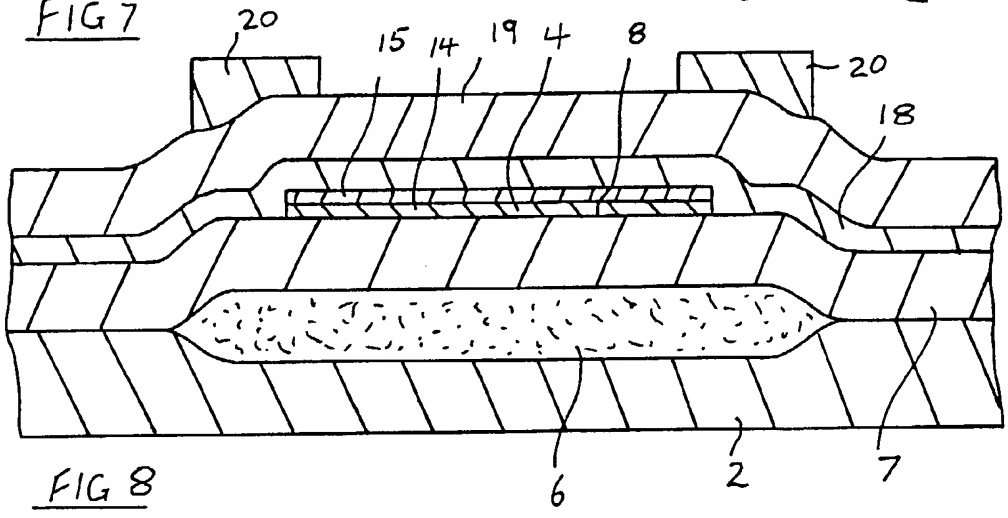

FIG 8

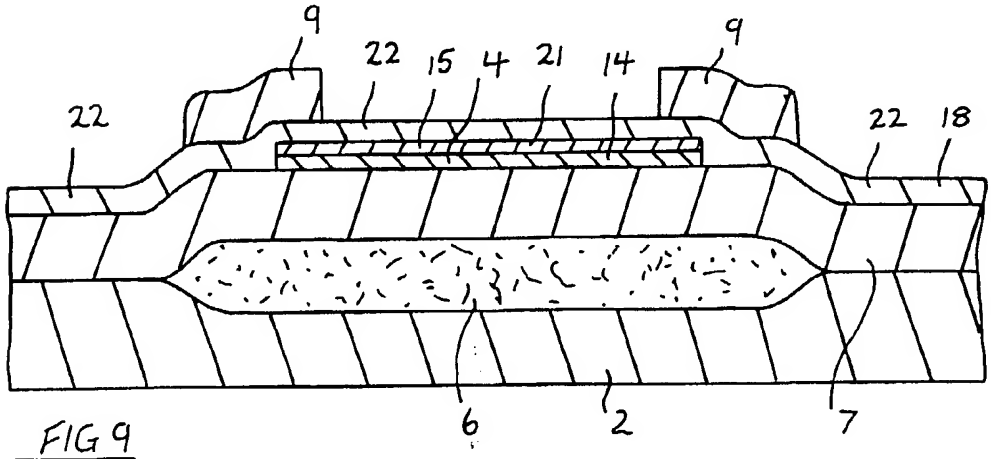

FIG 9

A METHOD FOR FORMING A THIN FILM RESISTOR ON AN IC WAFER

The present invention relates to a method for forming a film resistor on a semi-conductor integrated circuit wafer, and in particular though not limited to a method for forming a thin film resistor on a semi-conductor integrated circuit wafer. The invention also relates to a semi-conductor integrated circuit wafer with a film resistor formed according to the method.

In general, it has been found difficult to form thin film resistors in an integrated circuit wafer, and in particular it has been found difficult to form such thin film resistors in which matching and temperature co-efficient characteristics of the thin film resistors are preserved. Thin film resistors are susceptible to damage and destruction in subsequent processing steps in the manufacture of the wafer. In fact, the failure rate of integrated circuit wafers with thin film resistors formed using known methods is relatively high. In general, the thin film resistors are damaged and in many cases destroyed after the film resistors have been formed on the wafer during later steps in the processing of the wafer. In particular, it has been found that significant damage occurs to the film resistors when the next immediate conductive layer is being deposited and/or formed after the thin film resistors have been formed.

So far, no method has been devised which satisfactorily overcomes this problem. There is therefore a need for a method which permits the manufacture of a semi-conductor integrated circuit wafer with at least one film resistor which reduces the possibility of damage occurring to the film resistor after formation of the film resistors.

The present invention is directed towards providing such a method, and providing a semi-conductor integrated circuit wafer with at least one film resistor in which the possibility of damage occurring to the film resistor after formation of the film resistor is reduced.

According to the invention, there is provided a method for forming a film resistor on a semi-conductor integrated circuit wafer, the method comprising the steps of :

depositing a resistor layer of electrically conductive material for forming the film resistor on a surface of the wafer,

depositing a protective layer of electrically conductive, shielding material over the resistor layer,

depositing a first photoresist layer of photoresist material on the protective layer, and patterning the first photoresist layer to define the film resistor,

subjecting the wafer to a first etch to remove at least some of the protective layer from areas not protected by the first photoresist layer, and

subjecting the wafer to a radio frequency sputter etch to form the film resistor by removing the resistor layer and any remaining protective layer from the areas in which the protective layer has already been etched during the first etch.

In one embodiment of the invention, the protective layer is deposited to a depth of at least 150 Angstroms, and preferably to a depth of at least of 300 Angstroms, and advantageously to a depth of 400 Angstroms. In general, the protective layer would not be deposited to a depth of more than 1,000 Angstroms.

Advantageously, the protective layer is selected from any one or more of the following metals:

titanium,

tungsten.

In one embodiment of the invention, the first photoresist layer is removed after the first etch and before the radio frequency sputter etch.

In one embodiment of the invention, the first etch removes at least some of the protective layer not

protected by the first photoresist layer, and advantageously, the first etch removes substantially all of the protective layer not protected by the first photoresist layer. Preferably, the combined depth of the resistor layer and the protective layer remaining after the first etch should not exceed the depth of material removable by the radio frequency sputter etch.

Preferably, the resistor layer comprises a material selected from any one or more of the following materials:

silicon chrome,
nickel chrome,
titanium nitride.

Advantageously, the resistor layer is of silicon chrome.

In another embodiment of the invention, the radio frequency sputter etch is carried out in a non-reactive atmosphere. Advantageously, the radio frequency sputter etch is carried out in argon gas, and preferably, the radio frequency sputter etch is calibrated to etch at a rate of 200 Angstroms of silicon dioxide per minute.

In another embodiment of the invention, the first etch is a dry etch, and preferably, the first etch is a

plasma etch.

Alternatively, the first etch is carried out in a hydrogen peroxide bath, and preferably, the hydrogen peroxide is maintained at a temperature in the range of 40°C to 60°C, and advantageously, the hydrogen peroxide is maintained at a temperature of 50°C.

In a further embodiment of the invention, the film resistor is a thin film resistor, and preferably, the resistor layer is deposited to a depth of at least 10 Angstroms, and advantageously, the resistor layer is deposited to a depth in the range of 20 Angstroms to 60 Angstroms, and in preferred embodiment of the invention, the resistor layer is deposited to a depth of 30 Angstroms.

In one embodiment of the invention, the resistor layer is sputtered onto the surface of the wafer.

In another embodiment of the invention, the method further comprises the steps of depositing an electrically conductive material on the wafer to form an interconnect layer after the radio frequency sputter etch, depositing a second photoresist layer of photoresist material on the interconnect layer, and patterning the second photoresist layer to define a

conductor pattern to be formed from the interconnect layer, and subjecting the wafer to a third etch for removing portion of the interconnect layer not protected by the second photoresist layer for defining the conductors of the conductor pattern.

In a further embodiment of the invention, a diffusion barrier layer is deposited on the wafer after the radio frequency sputter etch and prior to the deposition of the interconnect layer. Preferably, the diffusion barrier layer is deposited to a depth of at least 500 Angstroms, and preferably, is deposited to a depth of at least 400 Angstroms. In general, the diffusion barrier layer would not be deposited to a depth of more than 1,500 Angstroms.

Additionally, the invention provides a semi-conductor integrated circuit wafer manufactured according to the method according to the invention.

Further, the invention provides a semi-conductor integrated circuit wafer comprising a film resistor, the film resistor having been formed by depositing a resistor layer of electrically conductive material for forming the film resistor on a surface of the wafer, depositing a protective layer of electrically conductive, shielding material over the resistor layer,

depositing and forming a first patterned photoresist layer of photoresist material on the protective layer, the first photoresist layer defining the film resistor, subjecting the wafer to a first etch to remove at least most of the protective layer from areas not protected by the first photoresist layer, and subjecting the wafer to a radio frequency sputter etch to form the film resistor by removing the resistor layer and any remaining protective layer from the areas in which the protective layer was already etched during the first etch.

The invention will be more clearly understood from the following description of a preferred embodiment thereof, given by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 is a typical plan view of portion of a semi-conductor integrated circuit wafer having a plurality of thin film resistors thereon according to the invention,

Fig. 2 is a cross sectional end view of the portion of the integrated circuit wafer of Fig. 1 on the line II-II of Fig. 1,

Figs. 3 to 9 are cross sectional end views similar

to Fig. 1 of the integrated circuit wafer at different stages of construction.

Referring to the drawings and initially to Figs. 1 and 2, there is illustrated portion of a semi-conductor integrated circuit wafer according to the invention indicated generally by the reference numeral 1 comprising a substrate 2 and a plurality of film resistors, namely, thin film resistors 4 formed thereon using a method according to the invention. Before describing the method for forming the thin film resistors 4, the relevant portions of the integrated circuit wafer 1 will first be described. The wafer 1 comprises the substrate 2 which is of silicon material in which MOS devices (not shown) and/or bi-polar transistors (not shown) are formed. The formation of such MOS devices and bi-polar transistors will be well known to those skilled in the art and it is not intended to describe them further. A field oxide layer 6 is formed on the substrate 2 between the MOS devices and bi-polar transistors. The formation of such an oxide layer will be well known to those skilled in the art. A dielectric layer 7 of chemical vapour deposition oxide is deposited over the wafer to a depth d_1 of approximately 7 KAngstroms. The thin film resistors 4 of silicon-chromium are formed on a surface 8 of the dielectric layer 7 over the field oxide layer

6 and extend between conductors 9 of aluminum alloy also formed on the dielectric layer 7 as will be described below.

Referring now to Figs. 3 to 9 the method for forming the thin film resistors 4 on the wafer 1 will now be described. The manufacture of the wafer up to and including the deposition of the dielectric layer 7 is carried out using known processes which will be well known to those skilled in the art, and accordingly it is not intended to describe the manufacture of the wafer up to this point in any further detail. A resistor layer 14 of silicon-chromium from which the thin film resistors 4 are formed is deposited on the surface 8 of the dielectric layer 7, see Fig. 3. The silicon-chromium is deposited to a depth d_2 of approximately 30 Angstroms by sputtering the silicon-chromium onto the surface 8.

A protective layer 15 of electrically conductive shielding material, namely titanium-tungsten alloy is deposited on the resistor layer 14 to protect the resistor layer 14 during part of the subsequent manufacturing process, see Fig. 3. In this embodiment of the invention, the titanium-tungsten alloy of the protective layer 15 comprises 90% titanium and 10% tungsten by weight. The titanium-tungsten alloy is

deposited by sputtering to a depth d_3 of approximately 500 Angstroms to form the protective layer 15. A first photoresist layer 16 of photoresist material is deposited over the protective layer 15, see Fig. 4, and the first photoresist layer 16 is patterned to define the thin film resistors 4. Such photoresist layers and patterning thereof will be well known to those skilled in the art.

After patterning of the first photoresist layer 16, the wafer 1 is then subjected to a first etch, in this case a dry, plasma etch for etching the protective layer 15 of titanium-tungsten alloy back to the resistor layer 14 in the areas not protected by the first photoresist layer 16, see Fig. 5. In this embodiment of the invention, the etching is carried out in a $CF_4 + O_2$ plasma in a Tegal 903 apparatus operating at a pressure of 150 mTORR at a power level of 100 watts at a frequency of 13.5 MHertz. The composition of the gas of the first etch is 96% CF_4 and 4% O_2 by volume of gas. The first etch is carried out for a time period of 90 seconds. By appropriately matching the power and time of the first etch, the position in the protective layer 15 at which the etch stops can be critically determined, although the precise point at which the first etch terminates is not particularly critical. Indeed, the first etch may etch into the resistor layer

14 with no adverse effects. If necessary, the first etch may terminate before the entire depth of the protective layer 15 has been etched. However, only a relatively shallow depth of the protective layer 15 not protected by the first photoresist layer 16 should remain after the first etch, and this is described in more detail below.

After the first etch, the first photoresist layer 16 is removed. On removal of the first photoresist layer 16, the wafer is then subjected to a radio frequency sputter etch which removes the resistor layer 14 in the areas which were already subjected to the first etch. If the first etch did not etch the areas of the protective layer 15 not protected by the first photoresist layer 16 completely away, in other words, if the first etch stopped before the protective layer 15 was etched back to the resistor layer 14, the radio frequency sputter etch first removes the remainder of the protective layer 15 which was already subjected to the first etch, and then proceeds to remove the resistor layer 14. The radio frequency sputter etch is set to remove the resistor layer 14 back to the dielectric layer 7. To avoid damage to other components on the wafer, it has been found preferable that the radio frequency sputter etch should be set to etch to a depth of not more than 100 Angstroms.

Therefore, where a shallow depth of protective layer 15 remains after the first sputter etch, it is important that the combined depth of the resistor layer 14 and the protective layer 15 remaining after the first etch should not exceed 100 Angstroms. In this embodiment of the invention, since the resistor layer 14 is deposited to a depth of 30 Angstroms, not more than 70 Angstroms of the protective layer 15 should remain in the areas not protected by the first photoresist layer 15 after the first etch.

At the end of the radio frequency sputter etch, the thin film resistors 4 are formed from the resistor layer 14 and are protected by the remaining portions of the protective layer 15 which cover the thin film resistors 4, see Fig. 6.

In this embodiment of the invention, the radio frequency sputter etch is carried out in a Varian 3290 sputtering apparatus in argon gas which is calibrated to remove approximately 200 Angstroms of silicon dioxide per minute. In this case, such a setting is achieved by setting the apparatus at a self-bias of 1,600 volts at a pressure of 5 to 7 mTorr and at a frequency of 13.56 MHertz. At this setting, the radio frequency sputter etch is carried out for not more than 30 seconds.

The radio frequency sputter etch also etches some of the titanium tungsten alloy material of the protective layer 15 which covers the portions of the resistor layer 14 which form the thin film resistors 4. However, provided the original depth of the protective layer 15 is sufficient, the radio frequency sputter etch does not etch completely through the protective layer 15 over the portions of the resistor layer 14 which form the thin film resistors 4. Thus, a sufficient depth of titanium-tungsten alloy material will remain in the protective layer 15 after the radio frequency sputter etch to protect the thin film resistors 4. In fact, it has been found that provided the protective layer 15 is originally deposited to a depth of at least 150 Angstroms, and preferably, at least 300 Angstroms, a sufficient depth of titanium-tungsten alloy material of the protective layer 15 remains after the radio frequency sputter etch protecting the film resistors 4.

As well as removing the resistor layer 14 and any of the protective layer 15 which may remain after the first etch, the radio frequency sputter etch also removes any oxides which may have built up on any of the electrically conductive metals of the wafer. Accordingly, good electrical contact is ensured between

the layers subjected to the radio frequency sputter etch and the layers which are subsequently deposited on these layers.

The wafer is now ready to receive an interconnect layer of aluminium alloy from which the conductors 9 are formed. However, to prevent spiking in areas where conductors of the interconnect layer are in contact with silicon, a diffusion barrier layer 18 of titanium-tungsten alloy similar to the protective layer 15 is deposited over the wafer, see Fig. 7. The titanium-tungsten alloy forming the diffusion barrier layer 18 is deposited to a depth d_4 of 1,000 Angstroms by sputtering. An interconnect layer 19 of aluminium alloy for forming the conductors 9 is deposited on the diffusion barrier layer 18, see Fig. 7. The aluminium alloy is deposited using conventional deposition methods to a depth d_5 of approximately 12 KAngstroms. A second photoresist layer 20 of photoresist material is deposited on the interconnect layer 19. The second photoresist layer 20 is patterned to define the conductor pattern to be formed in the interconnect layer 19 which includes the conductors 9 and any other conductors (not shown) to be formed from the interconnect layer 19, see Fig. 8. The second photoresist layer 20 and its method of patterning will be well known to those skilled in the art. The wafer

is subjected to a third etch to remove the portions of the interconnect layer 19 not protected by the second photoresist layer 20 to form the conductors 9. It is important that the protective layer 15 and the diffusion layer 18 of titanium-tungsten alloy should be resistant to the third etch, and furthermore, the third etch should not induce any post-etch corrosion or oxidisation. In this embodiment of the invention, the third etch is a $SiCl_2/BCl_3/Cl_2$ plasma etch and is carried out in an Electrotech Omega system using an $SiCl_2/BCl_3/Cl_2$ gas chemistry operating at 55 watt power level and at a pressure of 80 mTORR with a post-etch invacuo heat treatment of approximately 200°C for 17 seconds. The second photoresist layer 20 is then removed, see Fig. 9. When removing the second photoresist layer, it is important that the diffusion barrier layer should remain intact and should not be oxidised, otherwise, difficulty may be encountered when subsequently removing the diffusion barrier layer.

The wafer is immersed in a hydrogen peroxide bath and the remaining exposed portions 21 and 22 of the protective layer 15 and the diffusion barrier layer 18, respectively, are removed, see Fig. 9. In other words, the portions 21 and 22 of the layers 15 and 18 which are removed are those portions not beneath the conductors 9. The temperature of the hydrogen peroxide

is maintained at 50°C approximately.

A passivation layer (not shown) is then deposited on the wafer over the conductors 9, the thin film resistors 4 and the exposed portions of the dielectric layer 7. Such passivation layers and their methods of deposition will be well known to those skilled in the art.

The advantages of forming the thin film resistors according to the invention on the semi-conductor integrated circuit wafer are many. Tests on wafers on which thin film resistors have been formed using the method of the invention have shown that in virtually all the wafers no damage occurs to the thin film resistors during the formation of the conductors of the interconnect layer or during any other subsequent steps in the manufacture of the wafers. Further, it has been found that the resistance value of the thin film resistors remains relatively unaltered during the manufacture of the wafer, and accordingly, the resistance value of the thin film resistors may be maintained within tight tolerances. A particularly important advantage of the invention is achieved where a plurality of thin films are provided on a wafer and these are to be matched. It has been found that the important qualities of matching and temperature co-

efficient of the thin film resistors are preserved and remain relatively unaltered during the subsequent manufacturing process of the wafer. Furthermore, thin film resistors of desired resistance values are formed with little variation from the desired value, and as mentioned above, there is virtually no danger of any damage or destruction to the thin film resistors during the formation of the conductors of the interconnect layer.

It is believed that the majority of these advantages are achieved by providing the protective layer over the resistor layer. Indeed, it is believed that by providing the protective layer over the resistor layer, etching using a radio frequency sputter etch is permitted. It is believed that the radio frequency sputter etch gives a particularly good etch result, and also as discussed above, removes any oxides which may have built up on any of the electrically conductive metals of the wafer. This, thus, ensures good electrical contact between the layers subjected to the radio frequency sputter etch and the layers which are subsequently deposited on these layers.

It is believed that without the protective layer such a radio frequency sputter etch could not be used satisfactorily. It is believed that by depositing the

protective layer to a depth of not less than 150 Angstroms over the protective layer, a protective layer of sufficient depth will remain after the radio frequency sputter etch has been completed to protect the thin film resistors during subsequent processing of the wafer. Furthermore, should the first etch terminate before the protective layer has been etched down to the resistor layer, it is believed that provided the combined depth of the resistor layer and the remaining protective layer does not exceed 100 Angstroms, the radio frequency sputter etch may be used to remove the remaining protective layer and resistor layer without causing damage to other components of the wafer. It has, however, been found that excessive radio frequency sputter etching may cause damage to other components on the wafer. It is believed that provided the radio frequency sputter etch is calibrated to remove not more than 200 Angstroms of silicon dioxide per minute, and the time period for which the radio frequency sputter etch is carried out does not exceed 30 seconds, then damage to other components on the wafer is avoided.

While the method has been described as comprising the step of depositing the diffusion barrier layer of titanium-tungsten alloy, if desired the diffusion barrier layer may be dispensed with altogether.

Furthermore, while the diffusion barrier layer has been described as being of a similar composition to the protective layer, this is not essential, the diffusion barrier layer may be of any other compositions of material, and in many cases may contain titanium or tungsten but not both. Furthermore, the protective layer may be of any other electrically conductive material. Further, while the interconnect layer for forming the conductors has been described as being of aluminium alloy, it may be of any other suitable electrical conductive material. Further, while the thin film resistors have been described as being of silicon-chromium, they likewise may be of other suitable material without departing from the scope of the invention, for example, the resistor layer for forming the thin film resistors may be nickel chrome, titanium nitride or any other suitable material.

While the protective layer has been described as being of titanium-tungsten alloy, any other suitable electrically conductive, shielding materials could be used without departing from the scope of the invention. For example, the protective layer may be of titanium or tungsten, or may be of any other alloy of titanium or tungsten. Indeed, any other suitable electrically conductive metals may be used for the protective layer provided it can be removed after the conductors have

been formed.

While the thin film resistors have been described as being formed from a resistor layer deposited to a depth of 30 Angstroms, it is envisaged that the resistor layer may be of other depth. However, in general, it is envisaged that the depth of the resistor layer will be at least 10 Angstroms and in most cases will be within a range of 20 to 60 Angstroms. Needless to say, the method could also be used for forming thick film resistors and in which case the resistor layer would be deposited to a suitable depth which may be considerably greater than 500 Angstroms.

While a diffusion barrier layer has been described as being deposited over the protective layer to minimize the risk of spiking, the diffusion barrier layer may, if desired, be dispensed with altogether. Where a diffusion barrier layer is provided, it is envisaged that the diffusion barrier layer will be deposited to a depth in the range of 500 Angstroms to 1,500 Angstroms. However, diffusion barrier layers may be deposited to greater or lesser depths if desired or appropriate.

While the interconnect layer for forming the connectors has been described as being deposited to a depth of 12 KAngstroms, the interconnect layer may be deposited to

any other desired depth. However, in practice, it is envisaged that the interconnect layer will be deposited to a depth in the range of 4 Kangstroms to 40 KAngstroms.

Furthermore, while the protective layer has been described as being deposited to a depth of approximately 500 Angstroms, it is envisaged that the protective layer may be of any other suitable depth without departing from the scope of the invention. However, it is preferable that the protective layer should be deposited to a depth of not less than 150 Angstroms, and preferably should not be less than 300 Angstroms, and preferably, the maximum depth should not exceed 1,000 Angstroms.

Needless to say, while the first etch has been described as being a particular type of dry etch, other suitable dry etches may be used. Indeed, the first etch may be a wet etch if desired, and where a wet etch is used, it is envisaged that a particularly suitable wet etch would be a hydrogen peroxide etch, and preferably the hydrogen peroxide would be maintained at a temperature in the range of 40°C to 60°C and preferably at 50°C approximately. Needless to say, the parameters of the first etch may be varied without departing from the scope of the invention.

Needless to say, while the first etch has been described as being carried out in a Tegal 903 apparatus, the first etch could be carried out in any other suitable etching apparatus, and where the first etch is carried out in a Tegal 903 apparatus, other operating parameters besides those described could be used without departing from the scope of the invention.

Further, while the radio frequency sputter etch has been described as being carried out in a Varian 3290 sputtering apparatus, the radio frequency sputter etch may be carried out in any other suitable apparatus. Needless to say, where the radio frequency sputter etch is carried out in a Varian apparatus, other operating parameters may be used besides those described. Further, while it is preferable that the radio frequency sputter etch should be carried out in argon gas, it is not essential, any other non-reactive gas may be used without departing from the scope of the invention.

Further, it will be appreciated that while the remaining exposed portions 21 and 22 of the protective layer and the diffusion barrier layer 18 have been described as being removed in a hydrogen peroxide bath, any other suitable removing means may be used. Where a

hydrogen peroxide bath is used, it will be appreciated that the temperature of the hot hydrogen peroxide may be any desired temperature, but preferably should be in the range of 40°C to 60°C. However, it is important that whatever method is used for removing the exposed portions 21 and 22 of the protective layer and the diffusion barrier layer, such method should not affect the thin film resistors and the thin film resistors. In other words, the method should be non-reactive with the thin film resistors.

Further, it is envisaged that the post-etch invacuo heat treatment may be carried out at any suitable temperature up to 250°C for any suitable time period of up to 30 seconds.

While the third etch has been described as being carried out in an Electrotech Omega 2 system, any other suitable etch could be used without departing from the scope of the invention. However, it is important that the third etch should not etch the diffusion barrier layer 18 of titanium-tungsten alloy and also should not induce any post-etch corrosion or oxidisation. Needless to say, where an Electrotech Omega 2 system is used for the third etch, other operating parameters may be used without departing from the scope of the invention.

Additionally, if desired, a silicon layer may be deposited over the resistor layer prior to the deposition of the protective layer, although such a silicon layer is not essential. Where such a silicon layer is deposited, it is envisaged that it would be deposited to a depth in the range of 10 to 50 Angstroms, and preferably to a depth of 20 Angstroms. In general, the silicon layer would not be etched away, but would remain over the thin film resistors 4 after manufacture of the wafer had been completed. It is believed that the provision of such a silicon layer, in certain cases, may assist in subsequent trimming of the thin film resistors should this be necessary after manufacture of the wafer has been completed.

While the method of the invention has been described as forming a plurality of thin film resistors, the method may be used for forming an integrated circuit wafer with a single thin film resistor or any other single film resistor, or film resistors.

Needless to say, a dielectric layer of other material may be used if desired and the dielectric layer may be deposited to any other suitable depth without departing from the scope of the invention. Indeed, the dielectric layer may be dispensed with.

Further, while the resistors have been described as being formed over an oxide layer in the substrate, this is not necessary, the resistors may be formed at any other suitable or desired location on the substrate.

While the first photoresist layer has been described as being removed prior to the radio frequency sputter etch, while this is preferable, it is not essential. The first photoresist layer may be removed at any other desired stage in the method according to the invention.

CLAIMS

1. A method for forming a film resistor on a semiconductor integrated circuit wafer, the method comprising the steps of :

depositing a resistor layer of electrically conductive material for forming the film resistor on a surface of the wafer,

depositing a protective layer of electrically conductive, shielding material over the resistor layer,

depositing a first photoresist layer of photoresist material on the protective layer, and patterning the first photoresist layer to define the film resistor,

subjecting the wafer to a first etch to remove at least some of the protective layer from areas not protected by the first photoresist layer, and

subjecting the wafer to a radio frequency sputter etch to form the film resistor by removing the resistor layer and any remaining protective layer from the areas in which the protective layer has already been etched during the first etch.

2. A method as claimed in Claim 1 in which the protective layer is deposited to a depth of at least 150 Angstroms.

3. A method as claimed in Claim 1 or 2 in which the protective layer is deposited to a depth of at least of

300 Angstroms.

4. A method as claimed in Claim 3 in which the protective layer is deposited to a depth of at least 400 Angstroms.

5. A method as claimed in Claim 4 in which the protective layer is deposited to a depth of not more than 1,000 Angstroms.

6. A method as claimed in any preceding claim in which the protective layer is selected from any one or more of the following metals:

titanium,

tungsten.

7. A method as claimed in any preceding claim in which the protective layer is an alloy of titanium and tungsten.

8. A method as claimed in any preceding claim in which the protective layer is a titanium tungsten alloy comprising 90% titanium and 10% tungsten by weight.

9. A method as claimed in any preceding claim in which the first photoresist layer is removed after the first etch and before the radio frequency sputter etch.

10. A method as claimed in any preceding claim in which the first etch removes at least some of the protective layer not protected by the first photoresist layer, and the combined depth of the resistor layer and the protective layer remaining after the first etch should not exceed the depth of material removable by the radio frequency sputter etch.

11. A method as claimed in any preceding claim in which the first etch removes substantially all of the protective layer not protected by the first photoresist layer.

12. A method as claimed in any preceding claim in which the resistor layer comprises a material selected from any one or more of the following materials:

silicon chrome,
nickel chrome,
titanium nitride.

13. A method as claimed in any preceding claim in which the resistor layer is of silicon chrome.

14. A method as claimed in any preceding claim in which the radio frequency sputter etch is carried out in a non-reactive atmosphere.

15. A method as claimed in any preceding claim in which the radio frequency sputter etch is carried out in argon gas.

16. A method as claimed in any preceding claim in which the radio frequency sputter etch is calibrated to etch at a rate of 200 Angstroms of silicon dioxide per minute.

17. A method as claimed in any preceding claim in which the radio frequency sputter etch is carried out at a self-bias of 1,600 volts for a time period of 30 seconds.

18. A method as claimed in any preceding claim in which the first etch is a dry etch.

19. A method as claimed in any preceding claim in which the first etch is a plasma etch.

20. A method as claimed in any preceding claim in which the first etch is a $CF_4 + O_2$ plasma etch.

21. A method as claimed in Claim 20 in which the composition of the plasma gas is 96% CF_4 and 4% O_2 by volume of the gas.

22. A method as claimed in any preceding claim in which the first etch is carried out in a Tegal 903 apparatus operating at a pressure of 150 mTORR at a power level of 100 watts at a frequency of 13.5 Hertz.

23. A method as claimed in any of Claims 1 to 17 in which the first etch is carried out in a hydrogen peroxide bath.

24. A method as claimed in Claim 23 in which the hydrogen peroxide is maintained at a temperature in the range of 40°C to 60°C.

25. A method as claimed in Claim 24 in which the hydrogen peroxide is maintained at a temperature of 50°C.

26. A method as claimed in any preceding claim in which the film resistor is a thin film resistor.

27. A method as claimed in Claim 26 in which the resistor layer is deposited to a depth of at least 10 Angstroms.

28. A method as claimed in Claim 27 in which the resistor layer is deposited to a depth in the range of

20 Angstroms to 60 Angstroms.

29. A method as claimed in Claim 28 in which the resistor layer is deposited to a depth of 30 Angstroms.

30. A method as claimed in any preceding claim in which the resistor layer is sputtered onto the surface of the wafer.

31. A method as claimed in any preceding claim in which the method further comprises the steps of:

depositing an electrically conductive material on the wafer to form an interconnect layer after the radio frequency sputter etch,

depositing a second photoresist layer of photoresist material on the interconnect layer, and patterning the second photoresist layer to define a conductor pattern to be formed from the interconnect layer, and

subjecting the wafer to a third etch for removing portion of the interconnect layer not protected by the second photoresist layer for defining the conductors of the conductor pattern.

32. A method as claimed in Claim 31 in which the interconnect layer is an aluminium alloy.

33. A method as claimed in Claims 31 or 32 in which a diffusion barrier layer is deposited on the wafer after the radio frequency sputter etch and prior to the deposition of the interconnect layer.

34. A method as claimed in Claim 33 in which the diffusion barrier layer is deposited to a depth of at least 500 Angstroms.

35. A method as claimed in Claim 34 in which the diffusion barrier layer is deposited to a depth of not more than 1,500 Angstroms.

36. A method as claimed in any of Claims 33 to 35 in which the diffusion barrier layer is of titanium tungsten alloy material.

37. A method as claimed in Claims 33 to 35 in which the portion of the diffusion barrier layer not covered by the conductors is removed.

38. A method as claimed in any of Claims 31 to 37 in which the portion of the protective layer not covered by the conductors is removed.

39. A method as claimed in Claim 38 in which the protective layer and diffusion barrier layer are

removed by immersing the wafer in a hydrogen peroxide bath.

40. A method as claimed in Claim 38 or 39 in which a passivation layer is deposited on the wafer after the portions of the protective and diffusion barrier layers have been removed.

41. A method as claimed in any of Claims 31 to 40 in which the interconnect layer is deposited to a depth in the range of 4 KAngstroms to 40 KAngstroms.

42. A method as claimed in Claim 41 in which the interconnect layer is deposited to a depth of 12 KAngstroms.

43. A method as claimed in any of Claims 31 to 42 in which the third etch for etching the interconnect layer is a dry etch and is terminated when the interconnect layer has been fully etched back.

44. A method as claimed in any of Claims 31 to 43 in which the third etch is carried out in an Electrotech Omega 2 system using an $SiCl_2/BCl_3/Cl_2$ operating at a power of 55 watts and at a pressure of 80 mTORR.

45. A method as claimed in any preceding claim in

which the wafer is subjected to a post-etch invacuo heat treatment at a temperature of up to 250°C for a time period of up to 30 seconds.

46. A method as claimed in any preceding claim in which a dielectric layer is deposited on the wafer to form a surface for the reception of the resistor layer.

47. A method as claimed in Claim 46 in which the dielectric layer is deposited after MOS and/or bi-polar transistors have been formed in the wafer.

48. A method as claimed in any preceding claim in which a plurality of film resistors are simultaneously formed from the resistor layer.

49. A method for forming a film resistor on a semi-conductor integrated circuit wafer, the method being substantially as described herein with reference to and as illustrated in the accompanying drawings.

50. A semi-conductor integrated circuit wafer manufactured according to the method of any of Claims 1 to 49.

51. A semi-conductor integrated circuit wafer comprising a film resistor, the film resistor having

been formed by depositing a resistor layer of electrically conductive material for forming the film resistor on a surface of the wafer, depositing a protective layer of electrically conductive, shielding material over the resistor layer, depositing and forming a first patterned photoresist layer of photoresist material on the protective layer, the first photoresist layer defining the film resistor, and subjecting the wafer to a first etch to remove at least most of the protective layer from areas not protected by the first photoresist layer, subjecting the wafer to a radio frequency sputter etch to form the film resistor by removing the resistor layer and any remaining protective layer from the areas in which the protective layer was already etched during the first etch.

52. A wafer as claimed in Claim 51 in which the protective layer is deposited to a depth of at least of 150 Angstroms.

53. A wafer as claimed in Claim 51 or 52 in which the protective layer is deposited to a depth of not more than 1,000 Angstroms.

54. A wafer as claimed in any of Claims 51 to 53 in which the protective layer is selected from any one or

more of the following metals:

titanium,

tungsten.

55. A wafer as claimed in any of Claims 51 to 54 in which the protective layer is an alloy of titanium and tungsten.

56. A wafer as claimed in any of Claims 51 to 55 in which the protective layer is a titanium tungsten alloy comprising 90% titanium and 10% tungsten by weight.

57. A wafer as claimed in any of Claims 51 to 56 in which the first photoresist layer is removed after the first etch and before the radio frequency sputter etch.

58. A wafer as claimed in any of Claims 51 to 57 in which the wafer comprises conductors of electrically conductive material connecting the film resistor to another component of the wafer.

59. A wafer as claimed in Claim 58 in which the conductor is formed by depositing an interconnect layer of electrically conductive material over the wafer, and etching the interconnect layer to form the conductor.

60. A wafer as claimed in Claim 58 or 59 in which a

diffusion barrier layer is provided between the film resistor and the conductor.

61. A semi-conductor integrated circuit wafer comprising a film resistor, the semi-conductor integrated circuit wafer being substantially as described herein with reference to and as illustrated in the accompanying drawings.

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